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<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional) 075834.00064	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on <u>April 3, 2006</u> Signature <u><i>Amy L. Mitchell</i></u> Typed or printed name <u>Amy L. Mitchell</u>		Application Number  09/821,636	Filed  March 29, 2011
		First Named Inventor  Hiroyuki Ikeda	
		Art Unit  2811	Examiner  Thien F. Tran
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.  This request is being filed with a notice of appeal.  The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>45,219</u> <input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____		<u><i>Paige A. Kitzinger</i></u> Signature Paige A. Kitzinger Typed or printed name 312-704-1890 Telephone number April 3, 2006 Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			
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This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO in process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Appl. No.:** 09/821,636  
**Applicant:** Hiroyuki Ikeda  
**Filed:** March 29, 2001  
**TC/A.U.:** 2811  
**Examiner:** Thien F. Tran  
**Docket No.:** 075834.00064  
**Customer No.:** 33448

**Confirmation No.:** 5712**CERTIFICATION OF TELEFACSIMILE  
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I hereby certify that this paper is being facsimile  
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Amy Mitchell

**PRE-APPEAL BRIEF REQUEST FOR REVIEW ACCOMPANYING  
NOTICE OF APPEAL**

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S I R:

**ERRORS IN THE PRIOR REJECTION**

Consistent with the Review Requirements for identification of clear errors, Applicants note the following:

- I. The prior art fails to anticipate a dual gate transistor comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode when the first electrode gate electrode receives a second control voltage.
- II. The prior art fails to teach or suggest a dual gate transistor comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode when the first electrode gate electrode receives a second control voltage.

Appl. No. 09/821,636  
Reply to Office Action of November 2, 2005

#### REMARKS

##### A. The §102 Prior Art Rejection Is Improper

Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 3 and 39 – 41 under 35 U.S.C. §102(b). Examiner has rejected these claims in view of the cited prior art reference of *Kubota et al.* (U.S. Patent No. 5,808,595).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In their August 12<sup>th</sup>, 2005 Amendment, Applicants added the further limitation that the second threshold adjustment voltage be different than the first threshold adjustment voltage. This amendment was directed toward the fact that the circuit driver in the current apparatus does not apply a constant voltage to the second/V<sub>th</sub> adjustment gate. Rather, the threshold adjustment voltage applied differs between when the dual-gated transistor is turned on and when it is turned off (based upon a voltage applied to the first gate electrode being more than the effective V<sub>th</sub> of the device).

In the Office Action mailed on November 2, 2005, the Examiner took the position that the *Kubota* disclosed such a circuit in col. 13, lines 27 – 38 and in Figure 4. In the Response to Arguments section, the Examiner stated that “Applicant's arguments with respect to claims 1 – 3 and 39 – 41 have been considered but are moot in view of the new ground(s) of rejection.” Applicants note that the Examiner asserted the same reference in the March 28, 2005 rejection, in which the Examiner stated that “the claim does not require the first threshold adjustment voltage to the second gate electrode during off state to be different from the second threshold adjustment voltage to the

Appl. No. 09/821,636  
Reply to Office Action of November 2, 2005

second gate electrode during on state, [therefore], *Kubota* ... reads on the means as claimed." It is the Applicant's position that *Kubota* fails to anticipate exactly what is currently claimed, a second threshold adjustment voltage different than a first threshold adjustment voltage.

As noted above, the Federal Circuit has made clear that the prior art in a §102 rejection must teach *each and every element* of the claimed invention. Here, the Examiner continues to assert a §102 rejection, while the reference clearly teaches the application of a constant voltage to the second/ $V_{th}$  adjustment gate.

More specifically, Applicants note that the section of the prior art reference that the Examiner relies upon (Column 13, lines 27 – 38) merely details the well-known fact that a change in the voltage applied to the second gate of a dual-gated transistor will effect the threshold voltage of the transistor. Figure 4 shows that the application of voltage of -20V to the second electrode causes a shift in the threshold voltage of the transistor of approximately 2.5V when compared to the application of no bias voltage to the second electrode. This figure merely discloses the effect of changing the voltage applied to the second gate transistor (i.e., a range of operation of the transistor). Most importantly, the reference never discloses the variation of the voltage applied to the second gate during circuit operation. Rather, the reference actually teaches away from it. As clearly indicated in Column 12, lines 30 – 31, and throughout the remainder of the specification, the reference teaches that a constant voltage should be applied to the second gate electrode during circuit operation.

In light of the foregoing arguments and Federal Circuit caselaw, Applicants submit that 35 U.S.C. §102 rejection must be withdrawn, and claims 1 – 3 and 39 – 41 placed in condition for allowance.

Appl. No. 09/821,636  
Reply to Office Action of November 2, 2005

**B. The §103 Prior Art Rejection Is Improper**

Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 3 and 39 – 41 under 35 U.S.C. §103(a). Examiner has rejected these claims in view of the cited prior art reference of *Kubota et al.* (U.S. Patent No. 5,808,595).

Under Section 2143 of the MPEP, in order to establish a prima facie case of obviousness, the Examiner must meet three basic criteria. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." *MPEP §2143 rev. 3* (August, 2005). Applicants' assert that the Examiner has failed to establish a prima facie case of obviousness for at least the reason that the prior art reference fails to teach or suggest all of the claim limitations.

As discussed above, *Kubota* fails to teach or suggest the application of a second threshold adjustment voltage different than a first threshold adjustment voltage.

In light of the foregoing, Applicants submit that 35 U.S.C. §103 rejection must be withdrawn, and all remaining claims placed in condition for allowance.

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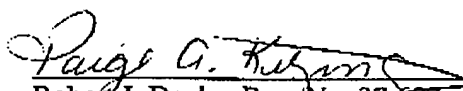
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Appl. No. 09/821,636

Reply to Office Action of November 2, 2005

Respectfully submitted,

Date: 4/3/06

  
Robert J. Depke, Reg. No. 37,607  
Paige A. Kitzinger, Reg. No. 43,219  
**TREXLER, BUSHNELL, CIANGIORGI  
BLACKSTONE & MARR, LTD.**  
105 W. Adams Street, 36<sup>th</sup> Floor  
Chicago, Illinois 60603  
Tel: (312) 704-1890  
**Attorney for Applicants**

page 5 of 5